CLAIMS:

1. A method of forming a capacitor comprising the following steps:

providing a node to which electrical connection to a first capacitor plate is to be made;

providing a first layer of material over the node, the first layer of material being selectively etchable relative to the node;

providing a second layer of material over the first layer, the second layer of material being selectively etchable relative to the first layer of material and being electrically conductive;

providing a first masking layer over the second layer of material;

etching a first opening into the first masking layer over the node;

providing a second masking layer over the first masking layer to a thickness which less than completely fills the first opening;

anisotropically etching the second masking layer to define a spacer received laterally within the first opening and thereby defining a second opening relative to the first masking layer which is smaller than the first opening;

after anisotropically etching the second masking layer, etching unmasked first masking layer material away;

after anisotropically etching the second masking layer, selectively anisotropically etching the second layer of material relative to the first layer of material;

after etching the second layer material, selectively etching the first layer of material relative to the node to effectively extend the second opening to the node and define an outline of the first capacitor plate using the spacer as an etching mask;

plugging the extended second opening with an electrically conductive plugging material, the plugging material electrically interconnecting the node and second layer;

after extending the second opening to the node, selectively isotropically etching the first layer material relative to the second layer material; and

providing a capacitor dielectric layer and a conductive second capacitor plate layer over the conductive second layer.

2. The method of forming a capacitor of claim 1 wherein the first opening is provided to have a minimum opening width equal to the minimum capable photolithographic feature dimension at the time of fabrication, the second opening thereby having a minimum opening width which is less than the minimum capable photolithographic feature dimension at the time of fabrication, the resultant plugging material plugging the second opening thereby having a minimum width which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

3. The method of forming a capacitor of claim 1 wherein the unmasked first masking layer is etched before extending the second opening to the node.

4. The method of forming a capacitor of claim 1 wherein the unmasked first masking layer is etched after extending the second opening to the node.

5. The method of forming a capacitor of claim 1 wherein only one photomasking step is utilized to define the first capacitor plate between the step of providing the node and the step of providing the capacitor dielectric layer.

6. The method of forming a capacitor of claim 1 wherein the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate.

7. The method of forming a capacitor of claim 1 wherein the first layer is electrically insulative.

8. The method of forming a capacitor of claim 1 wherein the first layer predominately comprises SiO_2.

9. The method of forming a capacitor of claim 1 wherein the second layer material constitutes the same material as that of the node.

10. The method of forming a capacitor of claim 1 wherein the plugging material, the node and the second layer of material all constitute the same material.

11. The method of forming a capacitor of claim 1 wherein the second masking material comprises Si_3N_4.

12. The method of forming a capacitor of claim 1 further comprising after selectively etching the first layer, etching the spacer away.

13. The method of forming a capacitor of claim 1 wherein the step of selectively etching the first layer comprises anisotropically etching the first layer.

14. The method of forming a capacitor of claim 1 wherein,

the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate; and

the first layer is electrically insulative.

15. The method of forming a capacitor of claim 1 wherein,

the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate;

the first layer is electrically insulative; and

further comprising after selectively etching the first layer, etching the spacer away.

16. The method of forming a capacitor of claim 1 wherein,

the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate;

the first layer is electrically insulative;

further comprising after selectively etching the first layer, etching the spacer away; and

wherein the plugging material, the node and the second layer of material all constitute the same material.

17. The method of forming a capacitor of claim 1 comprising etching the first masking layer away before anisotropically etching the second layer material, and then further comprising:

providing a third masking layer over the spacer;

anisotropically etching the third masking layer to form a secondary spacer laterally outward of the first stated spacer; and

using said spacers collectively as an etching mask during the second and first layer etchings.

18. The method of forming a capacitor of claim 17 further comprising forming at least two of said capacitors, the two capacitors being adjacent one another and having a minimum spacing from one another which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

19. The method of forming a capacitor of claim 1 further comprising providing a plurality of alternating of the first and second layers outwardly relative to the node, and providing the first and second masking layers and first and second openings outwardly thereof;

the method further comprising alternatingly anisotropically etching the respective second and first layers to extend the second opening therethrough to the node; and

the step of isotropically etching the first layer material relative to the second layer material defining a plurality of laterally projecting electrically conductive second layer fins.

20. The method of forming a capacitor of claim 19 wherein only one photomasking step is utilized to define the first capacitor plate between the step of providing the node and the step of providing the capacitor dielectric layer.

21. The method of forming a capacitor of claim 19 wherein the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate.

22. The method of forming a capacitor of claim 19 wherein the first layer is electrically insulative.

23. The method of forming a capacitor of claim 19 wherein the plugging material, the node and the second layer material all constitute the same material.

24. The method of forming a capacitor of claim 19 further comprising after selectively etching the first layer, etching the spacer away.

25. The method of forming a capacitor of claim 19 comprising etching the first masking layer away before anisotropically etching the second layer material, and then further comprising:

providing a third masking layer over the spacer;

anisotropically etching the third masking layer to form a secondary spacer laterally outward of the first stated spacer; and

using said spacers collectively as an etching mask during the second and first layer etchings.

26. The method of forming a capacitor of claim 19 wherein,

the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate; and

the first layer is electrically insulative.

27. The method of forming a capacitor of claim 19 wherein, the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate; the first layer is electrically insulative; and

further comprising after selectively etching the first layer, etching the spacer away.

28. The method of forming a capacitor of claim 19 wherein, the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate; the first layer is electrically insulative;

further comprising after selectively etching the first layer, etching the spacer away; and

wherein the plugging material, the node and the second layer of material all constitute the same material.

29. A capacitor produced according to the method of claim 1.

30. A method of forming a capacitor comprising the following steps:

providing a node to which electrical connection to a first capacitor plate is to be made;

providing a layer of conductive material outwardly of the node;

providing a first masking layer over the conductive material layer;

etching a first opening into the first masking layer over the node;

providing a second masking layer over the first masking layer to a thickness which less than completely fills the first opening;

anisotropically etching the second masking layer to define a spacer received laterally within the first opening and thereby defining a second opening relative to the first masking layer which is smaller than the first opening;

after anisotropically etching the second masking layer, etching unmasked first masking layer material away;

after anisotropically etching the second masking layer, etching through the conductive material layer to extend the second opening to the node, the node and conductive layer being electrically isolated from one another after the conductive material layer etching;

plugging the extended second opening with an electrically conductive plugging material, the plugging material electrically interconnecting the node and conductive layer; and

providing a capacitor dielectric layer and a conductive second capacitor plate layer over the conductive layer.

31. The method of forming a capacitor of claim 30 wherein the first opening is provided to have a minimum opening width equal to the minimum capable photolithographic feature dimension at the time of fabrication, the second opening thereby having a minimum opening width which is less than the minimum capable photolithographic feature dimension at the time of fabrication, the resultant plugging material plugging the second opening thereby having a minimum width which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

32. The method of forming a capacitor of claim 30 wherein only one photomasking step is utilized to define the first capacitor plate between the step of providing the node and the step of providing the capacitor dielectric layer.

33. The method of forming a capacitor of claim 30 wherein the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate.

34. The method of forming a capacitor of claim 30 wherein the conductive material layer constitutes the same material as that of the node.

35. The method of forming a capacitor of claim 30 wherein the plugging material, the node and the conductive material layer all constitute the same material.

36. The method of forming a capacitor of claim 30 wherein the second masking material comprises Si_3N_4.

37. The method of forming a capacitor of claim 30 further comprising after etching through the conductive material layer, etching the spacer away.

38. The method of forming a capacitor of claim 30 comprising etching the first masking layer away before etching through the conductive layer material, and then further comprising:

providing a third masking layer over the spacer;

anisotropically etching the third masking layer to form a secondary spacer laterally outward of the first stated spacer; and

using said spacers collectively as an etching mask during the second and first layer etchings.

39. A capacitor produced according to the method of claim 30.

40. A method of forming a capacitor comprising the following steps:

providing a node to which electrical connection to a first capacitor plate is to be made;

after providing the node, providing a finned lower capacitor plate in ohmic electrical connection with the node using no more than one photomasking step; and

providing a capacitor dielectric layer and a conductive second capacitor plate layer over the conductive layer.

41. The method of forming a capacitor of claim 40 wherein the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate.

42. The method of forming a capacitor of claim 40 wherein the finned lower capacitor plate constitutes the same material as that of the node.

43. A capacitor construction comprising:

a stem; and

at least two laterally opposed fins interconnected with and projecting laterally from the stem, the stem having a minimum width which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

44. A pair of adjacent capacitors fabricated relative to a semiconductor substrate, the adjacent capacitors having a minimum lateral spacing from one another which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

45. The capacitors of claim 44 wherein each comprises:

a stem; and

at least two laterally opposed fins interconnected with and projecting laterally from the stem, the stem having a minimum width which is less than the minimum capable photolithographic feature dimension at the time of fabrication.